WHAT IS CLAIMED IS:

1. A method for forming a low resistivity titanium silicide layer on a surface of at least one doped area of a silicon semiconductor substrate, said method comprising the steps of:

depositing a titanium layer on the surface of said at least one doped area of the silicon semiconductor substrate;

introducing an effective amount of a metallic element at least at the interface between the titanium layer and said at least one doped area of the silicon semiconductor substrate, the metallic element being chosen from the group consisting of indium, gallium, tin, and lead; and

sometime after the introducing step, performing a rapid thermal annealing of the titanium-coated silicon semiconductor substrate to form titanium silicide.

2. The method as defined in claim 1, wherein the metallic element is chosen from the group consisting of indium and gallium.

3. The method as defined in claim 1, wherein the metallic element is indium.

4. The method as defined in claim 1, wherein the effective amount of the metallic element is 1×10^{13} to 5×10^{14} atoms/cm^2.

5. The method as defined in claim 1, wherein the effective amount of the metallic element is 5×10^{13} to 5×10^{14} atoms/cm^2.

6. The method as defined in claim 1, wherein the effective amount of the metallic element is 5×10^{13} to 3×10^{14} atoms/cm^2.

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7. The method as defined in claim 1, wherein the introducing step includes the sub-step of depositing the effective amount of the metallic element on the surface of said at least one doped area of the silicon semiconductor substrate.

8. The method as defined in claim 1, wherein the introducing step includes the sub-step of implanting the effective amount of the metallic element into said at least one doped area of the silicon semiconductor substrate.

9. The method as defined in claim 8, wherein the implanting sub-step is performed before the depositing step.

10. The method as defined in claim 8, wherein in the implanting sub-step, the metallic element is implanted into said at least one doped area of the silicon semiconductor substrate to a depth of 5 to 25 nm.

11. The method as defined in claim 8, wherein in the implanting sub-step, the metallic element is implanted into said at least one doped area of the silicon semiconductor substrate to a depth of 8 to 20 nm.

12. The method as defined in claim 8, wherein in the implanting sub-step, the implantation energy is 5 to 30 keV.

13. The method as defined in claim 8, wherein in the implanting sub-step, the implantation energy is approximately 25 keV.

14. The method as defined in claim 1, wherein the introducing step is performed before the depositing step.

15. A method for fabricating a semiconductor device, said method comprising the steps of:

depositing a titanium layer on the surface of at least one doped area of a silicon semiconductor substrate;

introducing a predetermined amount of a metallic element at the interface between the titanium layer and said at least one doped area of the silicon semiconductor substrate, the metallic element being chosen from the group consisting of indium, gallium, tin, and lead; and

after the introducing step, performing a rapid thermal annealing of the silicon semiconductor substrate to form a low resistivity titanium silicide layer.

16. The method as defined in claim 15, wherein the metallic element is chosen from the group consisting of indium and gallium.

17. The method as defined in claim 15, wherein the predetermined amount of the metallic element is 1×10^{13} to 5×10^{14} atoms/cm^2.

18. The method as defined in claim 15, wherein the introducing step includes the sub-step of depositing the predetermined amount of the metallic element on the surface of said at least one doped area of the silicon semiconductor substrate.

19. The method as defined in claim 15, wherein the introducing step includes the sub-step of implanting the predetermined amount of the metallic element into said at least one doped area of the silicon semiconductor substrate.

20. The method as defined in claim 19, wherein in the implanting sub-step, the metallic element is implanted into said at least one doped area of the silicon semiconductor substrate to a depth of 5 to 25 nm.

21. The method as defined in claim 19, wherein in the implanting sub-step, the implantation energy is 5 to 30 keV.

22. A semiconductor device comprising:

a silicon semiconductor substrate; and

a low resistivity titanium silicide layer on a surface of at least one doped area of the silicon semiconductor substrate,

wherein there is 0.5 to 5‰ atoms of a metallic element at the interface between the titanium silicide layer and said at least one doped area of the silicon semiconductor substrate, the metallic element being chosen from the group consisting of indium, gallium, tin, and lead.

23. The semiconductor device as defined in claim 22, wherein the metallic element is chosen from the group consisting of indium and gallium.

24. The semiconductor device as defined in claim 22, wherein the metallic element is indium.

25. The semiconductor device as defined in claim 22, wherein there is 1×10^{13} to 5×10^{14} atoms/cm^2 of the metallic element at the interface between the titanium silicide layer and said at least one doped area of the silicon semiconductor substrate.

26. The semiconductor device as defined in claim 22, wherein the atoms of the metallic element are present in said at least one doped area of the silicon semiconductor substrate to a depth of at least 5 nm.

27. An information handling system including at least one semiconductor device that contains an integrated circuit, said semiconductor device comprising:

a silicon semiconductor substrate; and

a low resistivity titanium silicide layer on a surface of at least one doped area of the silicon semiconductor substrate,

wherein there is 0.5 to 5‰ atoms of a metallic element at the interface between the titanium silicide layer and said at least one doped area of the silicon semiconductor substrate, the metallic element being chosen from the group consisting of indium, gallium, tin, and lead.

28. The information handling system as defined in claim 27, wherein there is 1×10^{13} to 5×10^{14} atoms/cm^2 of the metallic element at the interface between the titanium silicide layer and said at least one doped area of the silicon semiconductor substrate.

29. The information handling system as defined in claim 27, wherein the atoms of the metallic element are present in said at least one doped area of the silicon semiconductor substrate to a depth of at least 5 nm.

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